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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,846	07/10/2003	Amanda C. Caswell	AUS920030426US1	1734

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,846	CASWELL ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *4,5,10,11,16 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-9,12-15,and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendment filed on 12 June 2006.

2. Claims 4 – 5, 10 – 11, and 16 – 17 have been cancelled.

3. Claims 21 –24 have been added new.

Claim Objections

4. Claims 1 – 3, 6 – 9, 12 – 15, and 18 – 24, are objected to because of the following informalities:

5. In the claims 1 – 3, and 6, the preamble states, " the method for reducing scan power consumption ------" which is mismatch with the steps in the body of the claim, "partitioning----; providing enough clocking----; keeping track-------; and scanning all of the plurality of segments one segment at a time" in the body of claim. Here, the power consumption [P_{total}] for scanning the whole chain is remaining same by partitioning the chain into plurality of segments and scanning all of the plurality of segments [$P_{i,\ I=1,2,---n}$] one segment at a time [$P_{total} = P_1 + P_2 + ---- + P_n$]. Either an essential steps are missing to achieve the tangible results in the body of the claim or misleading preamble statement. It describes just scanning technique.

6. In the claims 7 – 9, and 12, the preamble states, " an apparatus for reducing scan power consumption ------" which is mismatch with the elements in the body of the claim, "partitioning----; providing enough clocking----; keeping track-------; and scanning all of the plurality of segments one segment at a time" in the body of claim. Here, the power consumption [P_{total}] for scanning the whole chain is remaining same by partitioning the chain into plurality of segments and scanning all of the plurality of

segments [$P_{i,\ I=1,2,---n}$] one segment at a time [$P_{total} = P_1 + P_2 + ---- + P_n$]. Either an essential elements are missing to achieve the tangible results in the body of the claim or misleading preamble statement. It describes just scanning technique.

7. In the claims 13 – 15 and 18, the preamble states, " A computer program product for reducing scan power consumption ------" which is mismatch with the computer program code in the body of the claim, "partitioning----; providing enough clocking----; keeping track-------; and scanning all of the plurality of segments one segment at a time" in the body of claim. Here, the power consumption [P_{total}] for scanning the whole chain is remaining same by partitioning the chain into plurality of segments and scanning all of the plurality of segments [$P_{i,\ I=1,2,---n}$] one segment at a time [$P_{total} = P_1 + P_2 + ---- + P_n$]. Either an essential program codes are missing to achieve the tangible results in the body of the claim or misleading preamble statement. It describes just scanning technique.

8. In the claims 19 – 20, and 24, the preamble states, " Scan circuitry for reducing scan power consumption ------" which is mismatch with the elements claimed in the body of the claim, "partitioning----; providing enough clocking----; keeping track-------; and scanning all of the plurality of segments one segment at a time" in the body of claim. Here, the power consumption [P_{total}] for scanning the whole chain is remaining same by partitioning the chain into plurality of segments and scanning all of the plurality of segments [$P_{i,\ I=1,2,---n}$] one segment at a time [$P_{total} = P_1 + P_2 + ---- + P_n$]. Either an essential components of scan circuitry are missing to achieve the tangible results in the

body of the claim or misleading preamble statement. It describes just scanning technique.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 – 3, 6 – 9, 12 – 15, and 18 – 24, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Saxena et al. [hereinafter as Saxena], US Patent 6, 766, 487 B2 [cited and used in previous office action].

10. As to claim 1, Saxena discloses a low power scan architecture and method for reducing scan power consumption when unloading and restoring [load] content of a processor having one or more scan chains [col. 16, lines 26 – 31], the method comprising the steps of:

a. partitioning at least one scan chain [scan path] into a plurality of segments [scan segments A, B, C] [col. 4, lines 39 – 67, col. 15, lines 47 – 51, col. 16, lines 16 – 20] comprising one or more segments [A, B] of a predetermined [33 bits] length [equal number of scan cells/bits] and an offset segment [C, 31 bits][col. 4, lines 39 – 67, col. 5,

lines 1 – 16, col. 9, lines col. 10, lines 15 – 56, col. 15, lines 47 – 51, col. 16, lines 16 – 20, col. 21, lines 44 – 62];

b. providing enough clocking [timing by counting number of pulses] to scan all bits in the plurality of segments [A, B, C][col. 6, lines 12 – 65, col. 10, lines 40 – 56, col. 22, lines 5 – 16, fig. 4, 8, and 25];

c. keeping track [by monitoring counter output] of the predetermined lengths [33 bits], an order [when to start and stop scan operation of A, B, and C] of the segments [A, B][col. 9, lines 33 – 60, col. 10, lines 40 – 56], and the offset segment [C][col. 10, lines 40 – 56]; and

d. scanning all of the plurality of segments [A, B, C] one segment [steps 604, 606, and 608] at a time [col. 13, lines 52 – 57, fig. 6, 8, 13, 16 – 27] [col. 3, lines 35 – 55, col. 4, lines 43 – 67, col. 5, lines 17 – 52, col. 11, lines 47 – 67, col. 12, lines 1 – 30, col. 13, lines 32 – 57, col. 15, lines 9 – 67, col. 16, lines 1 – 46].

11. As to claim 7, Saxena discloses an apparatus [a low power scan architecture] for reducing scan power consumption when unloading and restoring [load] content of a processor having one or more scan chains [col. 16, lines 26 – 31], the apparatus comprising:

a. means for partitioning at least one scan chain [scan path] into a plurality of segments [scan segments A, B, C] [col. 4, lines 39 – 67, col. 15, lines 47 – 51, col. 16, lines 16 – 20] comprising one or more segments [A, B] of a predetermined [33 bits] length [equal number of scan cells/bits] and an offset segment [C, 31 bits][col. 4, lines

39 – 67, col. 5, lines 1 – 16, col. 9, lines col. 10, lines 15 – 56, col. 15, lines 47 – 51, col. 16, lines 16 – 20, col. 21, lines 44 – 62];

b. means for providing enough clocking [timing by counting number of pulses] to scan all bits in the plurality of segments [A, B, C][col. 6, lines 12 – 65, col. 10, lines 40 – 56, col. 22, lines 5 – 16, fig. 4, 8, and 25];

c. means for keeping track [by monitoring counter output] of the predetermined lengths [33 bits], an order [when to start and stop scan operation of A, B, and C] of the segments [A, B][col. 9, lines 33 – 60, col. 10, lines 40 – 56], and the offset segment [C][col. 10, lines 40 – 56]; and

d. means for scanning all of the plurality of segments [A, B, C] one segment [steps 604, 606, and 608] at a time [col. 13, lines 52 – 57, fig. 6, 8, 13, 16 – 27] [col. 3, lines 35 – 55, col. 4, lines 43 – 67, col. 5, lines 17 – 52, col. 11, lines 47 – 67, col. 12, lines 1 – 30, col. 13, lines 32 – 57, col. 15, lines 9 – 67, col. 16, lines 1 – 46].

12. As to claim 13, Saxena a computer program product [software product] for reducing scan power [low power scan] when unloading and restoring [loading] content of a processor having one or more [1-n] scan chains [paths], the computer program [software] product [col. 4, lines 28 – 35] having a medium with a computer program embodied thereon, the computer program comprising:

a. computer program code [software] for partitioning at least one scan chain into a plurality of segments comprising one or more segments of a predetermined [33 bits] length [equal number of scan cells/bits] and an offset segment [C, 31 bits][col. 4,

lines 39 – 67, col. 5, lines 1 – 16, col. 9, lines col. 10, lines 15 – 56, col. 15, lines 47 – 51, col. 16, lines 16 – 20, col. 21, lines 44 – 62];

b. computer program code [software] for providing enough clocking [by monitoring counter output] to scan all bits [33, 33, and 31 bits] in the plurality of segments [A, B, C][col. 22, lines 5 – 16];

c. computer program code [software] for keeping track of the predetermined length, an order of the segments, and the offset segment, and computer program code [software] for scanning all of the plurality of segments [A, B, C] one segment [steps 604, 606, and 608] at a time [col. 13, lines 52 – 57, fig. 6, 8, 13, 16 – 27] [col. 3, lines 35 – 55, col. 4, lines 43 – 67, col. 5, lines 17 – 52, col. 11, lines 47 – 67, col. 12, lines 1 – 30, col. 13, lines 32 – 57, col. 15, lines 9 – 67, col. 16, lines 1 – 46].

13. As to claim 19, Saxena discloses a scan circuitry [low power scan architecture] for reducing scan power consumption [low power scan architecture] when unloading and restoring [loading] content of a processor having one or more scan chains, the scan circuitry comprising:

a. a scan structure comprising one or more [1-n] scan chains [paths], wherein at least one of the one or more scan chain [scan path] is partitioned into a plurality of segments [A, B, C] comprising one or more segments [A, B] of a predetermined [33 bits] length [equal number of scan cells/bits] and an offset segment [C, 31 bits][col. 4, lines 39 – 67, col. 5, lines 1 – 16, col. 9, lines col. 10, lines 15 – 56, col. 15, lines 47 – 51, col. 16, lines 16 – 20, col. 21, lines 44 – 62];

b. a master conloller [504 adapter] coupled to the scan structure for providing enough clocking to scan all bits in the plurality of segments [col. 22, lines 5 – 16], tracking [by monitoring counter output] the predetermined length [33 bits], an order [when to start and stop scan operation of A, B, and C] of the segments [A, B][col. 9, lines 33 – 60, col. 10, lines 40 – 56], and the offset segment [C][col. 10, lines 40 – 56], and scanning all of the plurality of segments [A, B, C] one segment [steps 604, 606, and 608] at a time [col. 13, lines 52 – 57, fig. 6, 8, 13, 16 – 27]][col. 3, lines 35 – 55, col. 4, lines 43 – 67, col. 5, lines 17 – 52, col. 11, lines 47 – 67, col. 12, lines 1 – 30, col. 13, lines 32 – 57, col. 15, lines 9 – 67, col. 16, lines 1 – 46].

14. As to claims 2, 8, and 14, Saxena discloses one or more segments [scan paths] of a predetermined length [number of scan cells] including of equal length [equal number of scan cells/bits [col. 9, lines 20 – 25, col. 10, lines 15 – 20].

15. As to claims 3, 9, and 15, Saxena teaches the offset segment and is used to handle variations in length between the one or more scan chains [col. 10, lines 15 – 34].

16. As to claims 6, 12, and 18, Saxena teaches partitioning any remaining one or more of the one or more scan chains [scan path 1 – n] into a plurality of segments [A, B, C]; and scanning the plurality of segments one at a time [col. 11, lines 48 – 67, col. 12, lines 1 – 23, col. 13, lines 52 – 57].

17. As to claim 20, Saxena teaches scan circuitry [scan architecture] including an off-chip memory [204 D-FF, fig. 2] coupled to the master controller [504 adapter] for storing unloaded [scanned] content [output] of the processor [CPU-core] [col. 1, lines 20 – 36, col. 2, lines 3 – 20, fig. 2, 18 – 21].

18. As to claims 21 – 24, Saxena discloses a SCANENA signal with SCANACK to scan selected scan path segment, which inherently teaches to disable segments not to be scaned [unselected segments][col. 6, lines 12 – 48, col. 7, lines 12 – 15, fig. 7].

19. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

20. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Response to Arguments

21. Applicant's arguments regarding Kapur reference with respect to claims 1, 7, 13, and 19, have been considered but are moot in view of the new ground(s) of rejection.

22. Applicant's arguments regarding Saxena's reference filed on 12 June 2006 have been fully considered but they are not persuasive.

23. Applicant argues that neither Kapur nor Saxena individually or in combination suggest, teach or disclose "partitioning at least one scan chain into plurality of segments comprising one or more segments of predetermined length and an offset segment," and

"scanning all of the plurality of segments one segment at a time". The examiner disagrees. Saxena reads on the claimed limitations as described in rejection above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin C. Patel
July 10, 2006

LYNNE H. BROWNE
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